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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,976	10/21/2003	Glenn A. Rinne	9180-24	3798

7590 12/29/2005

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EXAMINER
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MATISIAK, JENNIFER E

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	<b>Application No.</b> 10/689,976	<b>Applicant(s)</b> RINNE, GLENN ET AL.	
	<b>Examiner</b> Jennifer Matisiak	<b>Art Unit</b> 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-61 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 54-60 is/are allowed.
- 6) ☒ Claim(s) 1-4, 7, 8, 21, 22, 25, 42, 43, 45-51 and 61 is/are rejected.
- 7) ☒ Claim(s) 5, 6, 9-20, 23-24, 26-41, 44, 52 and 53 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 February 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |  |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date: ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)            |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>2004/06/28</u> | 6) <input type="checkbox"/> Other: ____  |

**DETAILED ACTION**

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claim 61 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, "a third integrated circuit substrate mounted on the second integrated circuit substrate such that the second integrated circuit substrate is between the first and second integrated circuit substrates" is confusing because the position of the second substrate is self-referencing. Appropriate correction must be made.

***Specification***

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the limitations "a first array of interconnection structures on the first surface of the substrate wherein the first array of interconnection structures are arranged in a first pattern; a second array of interconnection structures on the second

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surface of the substrate wherein the second array of interconnection structures are arranged in a second pattern and wherein the second pattern is a mirror image of the first pattern", (emphasis added), as required in claim 54, and "a third array of interconnection structures on the first surface of the substrate spaced apart from the first array of interconnection structures wherein the third array of interconnection structures are arranged in a third pattern; a fourth array of interconnection structures on the second surface of the substrate spaced apart from the second array of interconnection structures wherein the fourth array of interconnection structures are arranged in a fourth pattern and wherein the fourth pattern is a mirror image of the third pattern", (emphasis added), as required in claim 57, are not adequately not described in the disclosure. Appropriate correction is required.

### ***Drawings***

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "wherein the second pattern is a mirror image of the first pattern", as required in claim 54, and "wherein the fourth pattern is a mirror image of the third pattern", as required in claim 57 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate

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prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Claim Rejections - 35 USC § 102***

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 3, 7, 8 and 61 are rejected under 35 U.S.C. 102(b) as being anticipated by Bozso et al. (US 5760478), hereinafter Bozso.

Regarding claim 1, Bozso discloses an electronic device (Fig 8, for example) comprising: a first electronic substrate (804 of Fig. 8, for example); a second electronic substrate (800 of Fig. 8) on the first electronic substrate; a third electronic substrate (802 of Fig. 8) on the second electronic substrate wherein the second electronic substrate is between the first and third electronic substrates; a first electrical and

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mechanical connection (808 of Fig. 8) between the first and third electronic substrates wherein the first electrical and mechanical connection bypasses the second substrate; and a second electrical and mechanical connection (806 of Fig. 8) between the second and third electronic substrates.

Regarding claim 2, Bozso discloses an electronic device wherein the second electronic substrate is offset relative to the first and third electronic substrates so that the first and third electronic substrates extend beyond an end of the second electronic substrate (Fig. 8).

Regarding claim 3, Bozso discloses an electronic device wherein the first electrical and mechanical connection is between portions of the first and third electronic substrates extending beyond the end of the second electronic substrate (Fig. 8).

Regarding claim 7, Bozso discloses an electronic device wherein the first electrical and mechanical connection comprises a first conductive bump between the first and third electronic substrates and wherein the second electrical and mechanical connection comprises a second conductive bump between the second and third electronic substrates (Fig. 8).

Regarding claim 8, Bozso discloses an electronic device wherein the first conductive bump has a greater volume than the second conductive bump (Fig. 8).

Regarding claim 61, Bozso discloses an electronic device comprising: a first integrated circuit substrate (804 of Fig. 8); a second integrated circuit substrate (800 of Fig. 8) mounted on the first integrated circuit substrate; a third integrated circuit substrate (802 of Fig. 8) mounted on the second integrated circuit substrate such that

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the second integrated circuit substrate is between the first and second integrated circuit substrates; at least one large bump providing electrical and mechanical connection (808 of Fig. 8) between the first and third integrated circuit substrates; and at least one small bump (806 of Fig. 8) providing electrical and mechanical connection between the second and third integrated circuit substrates wherein the at least one large bump has a greater volume than the at least one small bump.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim 21-22 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Fogal et al. (US 6563205), hereinafter Fogal.

Regarding claim 21, Fogal discloses an electronic device comprising: a printed circuit board; a first electronic substrate (18 of Fig. 4, for example) on the printed circuit board (12 of Fig. 4 col 1, lines 39-41, 59-62, for example); a second electronic substrate (28 of Fig. 4) on the first electronic substrate wherein the first electronic substrate is between the printed circuit board and the second electronic substrate; and a third electronic substrate (54 of Fig. 4) on the second electronic substrate wherein the second electronic substrate is between the first and third electronic substrates, wherein the second electronic substrate is offset relative to the first and third electronic

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substrates so that the first and third electronic substrates extend beyond an end of the second electronic substrate.

Regarding claim 22, Fogal discloses an electronic device further comprising: a first electrical and mechanical connection between the first and third electronic substrates (50 of Fig. 4); and a second electrical and mechanical connection between the second and third electronic substrates (50 of Fig. 4).

Regarding claim 25, Fogal discloses an electronic device further comprising: a third electrical and mechanical connection between the first and second electronic substrates (50 of Fig. 4).

6. Claims 42, 43 and 45-49 are rejected under 35 U.S.C. 102(e) as being anticipated by Moden et al. (US 2005/0146010), hereinafter Moden.

Regarding claim 42, Moden discloses an electronic device (Fig. 1 as shown below, for example) comprising: a first electronic substrate (Fig. 1 as shown below) having opposing first and second

surfaces; a second electronic substrate on the first electronic substrate, the second electronic substrate having opposing first and second surfaces; a third electronic substrate, on the second electronic substrate, the third electronic

substrate having opposing first and second surfaces, wherein the second electronic substrate is between the first and third electronic substrates; and a signal path (24 of

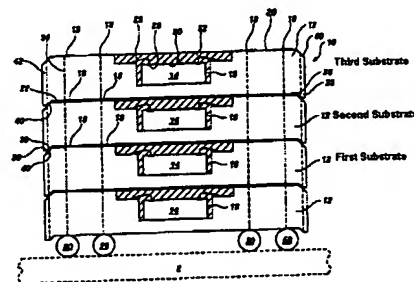


Fig. 1



Fig. 2, for example) extending along the first surface of the second electronic substrate (Fig. 1), to the second surface of the first electronic substrate (Fig. 1), along the second surface of the first electronic substrate (24 of Fig. 2 through 14 of Fig. 1), to the first surface of the third electronic substrate (Fig. 1), along the first surface of the third electronic substrate (24 of Fig. 2 through 14 of Fig. 1), and to the second surface of the second electronic substrate.

Regarding claim 43, Moden discloses an electronic device (Figs. 1 and 2) wherein the signal path comprises a first conductive trace (24 of Fig. 2 as aforementioned above) on the first surface of the second electronic substrate (as aforementioned above), a first electrical and mechanical connection between the first surface of the second electronic substrate and the second surface of the first electronic substrate (18 of Fig. 1), a second conductive trace (24 of Fig. 2 as aforementioned above) on the second surface of the first electronic substrate, a second electrical and mechanical connection between the second surface of the first electronic substrate and the first surface of the third electronic substrate (18 of Fig. 1), a third conductive trace of the first surface of the third electronic substrate (24 of Fig. 2 as aforementioned above), and a third electrical and mechanical connection between the first surface of the third electronic substrate and the second surface of the second electronic substrate (18 of Fig. 1).

Regarding claim 45, Moden discloses an electronic device (device below substrate 2 of Fig. 4) wherein the first and third electronic substrates comprise integrated circuit devices (14 of Fig. 4), wherein the first side of the first

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(10 of Fig. 4) and third (10 of Fig. 4)

electronic substrates comprises a device side and wherein the second side of the first and third electronic substrates comprises a backside.

Regarding claim 46, Moden discloses an electronic device (Fig. 4) wherein the signal path is electrically coupled (18 of Fig. 4) to an electronic circuit of the third electronic substrate.

Regarding claim 47, Moden discloses an electronic device (Fig. 4) wherein the second electronic substrate comprises an integrated circuit device, wherein the first side of the second electronic substrate comprises a device side and wherein the second side of the second electronic substrate comprises a backside (14 of Fig. 4).

Regarding claim 48, Moden discloses an electronic device (Fig. 4) wherein the signal path is electrically coupled to an electronic circuit of the second electronic substrate and to an electronic circuit of the third electronic substrate (18 of Fig. 4).

Regarding claim 49, Moden discloses an electronic device (Fig. 1) wherein the first, second, and third electronic substrates comprise respective memory devices (para [0005], for example).

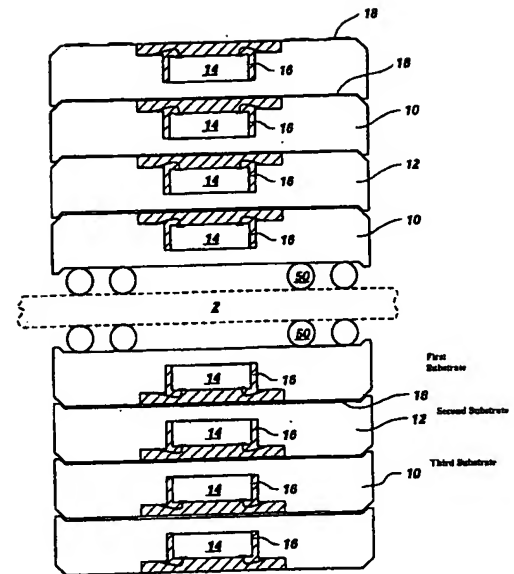


Fig. 4

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***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bozso, as applied to claim 1 above, in further view of Moden.

Regarding claim 4, Bozso discloses the limitation of claim 1 as divulged above. The difference between Bozso and the claimed invention is "a conductive trace providing an electrical coupling between the first and second electrical and mechanical connections." Moden discloses a conductive trace (24 of Fig. 2) on a surface of the third electronic substrate (Fig. 1) which provides an electrical coupling between the first and second electrical and mechanical connections as disclosed previously. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Bozso to include a conductive trace as a means for coupling the first and second mechanical connections since it is desirable to have a more efficient access to the electronic device on the die.

8. Claims 50-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moden.

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Regarding claim 50, Moden discloses the limitations of claim 42 as divulged above. Moden does not overtly disclose "a fourth electronic substrate on the third electronic substrate wherein the third electronic substrate is between the second and fourth electronic substrates; and wherein the signal path further extends along the second surface of the second electronic substrate, and to a first surface of the fourth electronic substrate." However, it is readily apparent to the ordinary artisan that the number of substrates having corresponding devices and signal paths thereon of the invention of Moden is not limitative to the explicit disclosure of Moden.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Moden by including a fourth electronic substrate on the third electronic substrate wherein the third electronic substrate is between the second and fourth electronic substrates since it is desirable to package as many integrated circuit devices in a single package as possible.

Additionally, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Moden by including a signal path further extending along the second surface of the second electronic substrate, and to a first surface of the fourth electronic substrate since it is desirable to reduce processing time by forming the same signal path for this assembly as on all other assemblies of the package disclosed by Moden.

Regarding claim 51, Moden discloses the limitations of claim 50 as divulged above. Moden does not explicitly disclose "wherein the signal path is electrically coupled with electronic circuits of the second and fourth substrates." However, it is

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readily apparent to the ordinary artisan that the signal path would be electrically coupled with electronic circuits of the second and fourth substrates in the same manner as set forth above. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Moden by including a signal path that is electrically coupled with electronic circuits of the second and fourth substrates since it is desirable to have the same signal pathways for all assemblies as disclosed by Moden.

***Allowable Subject Matter***

9. Claim 54-60 allowed. The following is a statement of reasons for the indication of allowable subject matter: regarding claim 54, the prior art on record whether applied alone or in combination thereof does not teach an electronic device as recited in the claim, particularly "wherein the second pattern is a mirror image of the first pattern".

10. Claims 5, 6, 9-20, 23-24, 26-41, 44, and 52-53 are objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer Matisiak whose telephone number is 571-272-2639. The examiner can normally be reached on Business Days 9:30a-6:30p EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 517-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JEM

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